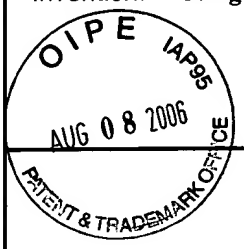
AF/2

TRANSMITTAL OF APPEAL BRIEF (Large Entity)	Docket No. ITL.0546US

In Re Application Of: **David K. Vavro**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
09/826,134	April 4, 2001	Tonia L. Meonske	21906	2181	2324

Invention: **Using a Plurality of Processing Elements (as Amended)**



COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **June 30, 2006**

The fee for filing this Appeal Brief is: **$500.00**

☒ A check in the amount of the fee is enclosed.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☒ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **20-1504**

☐ Payment by credit card. Form PTO-2038 is attached.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

Signature

Dated: **August 4, 2006**

Timothy N. Trop, Reg. No. 28,994
TROP, PRUNER & HU, P.C.
1616 S. Voss Road, Suite 750
Houston, TX 77057
713/468-8880 [Phone]
713/468-8883 [Fax]

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on

August 4, 2006
(Date)

Signature of Person Mailing Correspondence

Nancy Meshkoff

Typed or Printed Name of Person Mailing Correspondence

cc:

OIPE IAP95 AUG 08 2006 PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:	David K. Vavro	Art Unit:	2181
Serial No.:	09/826,134	Examiner:	Tonia L. Meonske
Filed:	April 4, 2001	Atty Docket:	ITL.0546US (P11105)
For:	Using a Plurality of Processing Elements (as Amended)	Assignee:	Intel Corporation

Mail Stop **Appeal Brief-Patents**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

08/09/2006 HWOLDGE1 00000025 09826134

01 FC:1402 500.00 OP

Date of Deposit: August 4 2006
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Nancy Meshkoff

TABLE OF CONTENTS

REAL PARTY IN INTEREST 3
RELATED APPEALS AND INTERFERENCES 4
STATUS OF CLAIMS 5
STATUS OF AMENDMENTS 6
SUMMARY OF CLAIMED SUBJECT MATTER 7
GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL 9
ARGUMENT 10
CLAIMS APPENDIX 12
EVIDENCE APPENDIX 15
RELATED PROCEEDINGS APPENDIX 16

REAL PARTY IN INTEREST

The real party in interest is the assignee Intel Corporation.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

Claims 1-17 (Rejected).

Claims 18-30 (Canceled).

Claims 1-17 are rejected and are the subject of this Appeal Brief.

STATUS OF AMENDMENTS

All amendments have been entered.

SUMMARY OF CLAIMED SUBJECT MATTER

In the following discussion, the independent claims are read on one of many possible embodiments without limiting the claims:

1. A method comprising:

providing a register (16, Figure 1) accessible by a plurality of central processing units (12a-e, Figure 1); and

indicating whether data in said register is available for a given central processing unit by providing different indicators (36, Figure 2) assigned to each of a plurality of central processing units (specification, page 6, lines 12-15) and causing the given central processing unit to reset its indicator when the data in said register is no longer useful to the given central processing unit (specification, page 8, line 25-page 9, line 2).

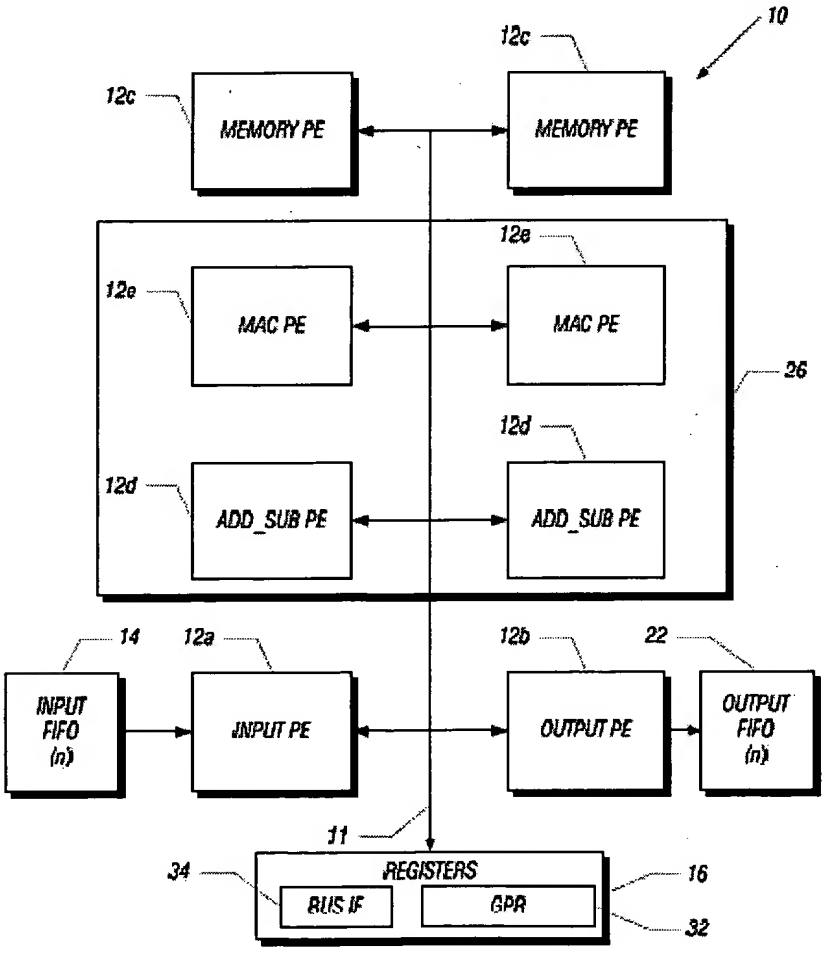


FIG. 1

11. A computer readable medium storing instructions that, when executed, enable a processor-based system to:

make a register (16, Figure 1) accessible by a plurality of central processing units (12a-e, Figure 1) in said system;

provide different indictors (36, Figure 2) for each of a plurality of central processing units (specification, page 6, lines 12-15);

indicate whether data in said register is available for a given processing unit (specification, page 8, lines 1-3); and

cause the given central processing unit to reset its indicator when data in the register is no longer useful for the given central processing unit (specification, page 8, line 25-page 9, line 2).

At this point, no issue has been raised that would suggest that the words in the claims have any meaning other than their ordinary meanings. Nothing in this section should be taken as an indication that any claim term has a meaning other than its ordinary meaning.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Do claims 1-17 fail to point out and distinctly claim the subject matter of the invention?

B. Do claims 1, 8, and 11-17 fail to produce a useful, concrete, and tangible result?

C. Are claims 1-17 anticipated by Chastain?

ARGUMENT

A. Do claims 1-17 fail to point out and distinctly claim the subject matter of the invention?

It is believed that the requested changes to the claims were made and therefore this rejection has been overcome.

B. Do claims 1, 8, and 11-17 fail to produce a useful, concrete, and tangible result?

It is believed that the requested changes to the claims were made and therefore this rejection has been overcome.

C. Are claims 1-17 anticipated by Chastain?

Claim 1 calls for providing different indicators assigned to each of a plurality of central processing units. The cited reference does no such thing. It is suggested that this is taught in column 8, lines 29-43 for the first time in the Advisory Action. Prior to that, hundreds of lines were cited with no explanation for the basis for the rejection.

The material cited in the Advisory Action does not suggest anything about providing an indicator that is different for each processor. To the contrary, each processor can access a fork block which is the dedicated region 000A-D shown in Figure 3. There is only the one fork block that is shown. It does not appear that there is any indicator specific to each processor. Nowhere is there any indicator to indicate which processor accessed the fork block.

Thus, contrary to the present system, it is not possible to know which processor accessed the fork block. This is not a problem in the cited reference, because in the cited reference only one processor acts at a time and all the other processors are idle. *See* column 5, lines 42-44. Thus not only does the cited reference fail to teach what is claimed, you would have no rationale to do what is claimed.

This claim also calls for causing a given central processing unit to reset its indicator when the data in the register is no longer useful to the given central processing unit. No effort has ever been made to point this element out and none has been found. There is no indicator for each processor and therefore there is no resetting of the indicator.

The rejection is woefully inadequate, failing to point out any of the claimed elements and citing a mass of material, or, in the case of the Advisory Action, a specific set of material that has no bearing on the claimed invention.

Therefore reversal would be appropriate.

Applicant respectfully requests that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

Date: August 4, 2006

Timothy N. Trop, Reg. No. 28,994
TROP, PRUNER & HU, P.C.
1616 S. Voss Road, Suite 750
Houston, TX 77057
713/468-8880 [Phone]
713/468-8883 [Fax]

Attorneys for Intel Corporation

CLAIMS APPENDIX

The claims on appeal are:

1. A method comprising:

providing a register accessible by a plurality of central processing units; and

indicating whether data in said register is available for a given central processing unit by providing different indicators assigned to each of a plurality of central processing units and causing the given central processing unit to reset its indicator when the data in said register is no longer useful to the given central processing unit.

2. The method of claim 1 including indicating for each of a plurality of central processing units whether the data is available for a given central processing unit.

3. The method of claim 2 including requiring a central processing unit to wait to execute an instruction until the data it needs to execute the instruction is available in one or more registers.

4. The method of claim 3 including providing a bit for each item of data indicating whether a given central processing unit can access that data.

5. The method of claim 4 including resetting said bit when said data is accessed by a given central processing unit.

6. The method of claim 1 including preventing any central processing unit from writing data to said register until all of the indicators for the plurality of central processing units indicate that the data is no longer useful to any other central processing unit.

7. The method of claim 6 including indicating the central processing unit which will utilize the data written into the register.

8. The method of claim 1 includes causing a plurality of central processing units to access a register at the same time.

9. The method of claim 1 including providing specialized central processing units for mathematical operations and for memory.

10. The method of claim 1 including providing an input central processing unit, an output central processing unit and coupling said input, output and specialized central processing units to said register through a cross-bar connection.

11. A computer readable medium storing instructions that, when executed, enable a processor-based system to:

make a register accessible by a plurality of central processing units in said system;

provide different indictors for each of a plurality of central processing units;

indicate whether data in said register is available for a given processing unit; and

cause the given central processing unit to reset its indicator when data in the register is no longer useful for the given central processing unit.

12. The medium of claim 11 further storing instructions that cause the processor-based system to determine whether data is available in a register for a particular processing unit.

13. The medium of claim 12 further storing instructions that cause the processor-based system to prevent execution of an instruction until the data needed to execute the instruction is available in one or more registers.

14. The medium of claim 13 further storing instructions that cause the processor-based system to check a bit in said register for each item of data indicating whether a processing unit can access said data.

15. The medium of claim 14 further storing instructions that cause the processor-based system to reset said bit when said data is accessed by a processing unit.

16. The medium of claim 15 further storing instructions that cause the processor-based system to avoid writing said data to said register until all the bits indicate that the data is no longer useful to any other processing unit.

17. The medium of claim 16 further storing instructions that cause the processor-based system to indicate which processing unit will utilize the data written into the register by another processing unit.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.